Fig. 1

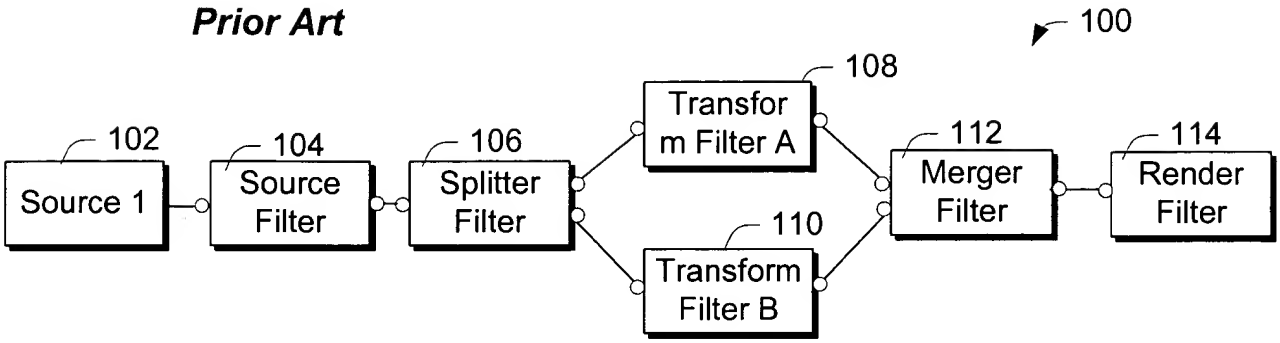
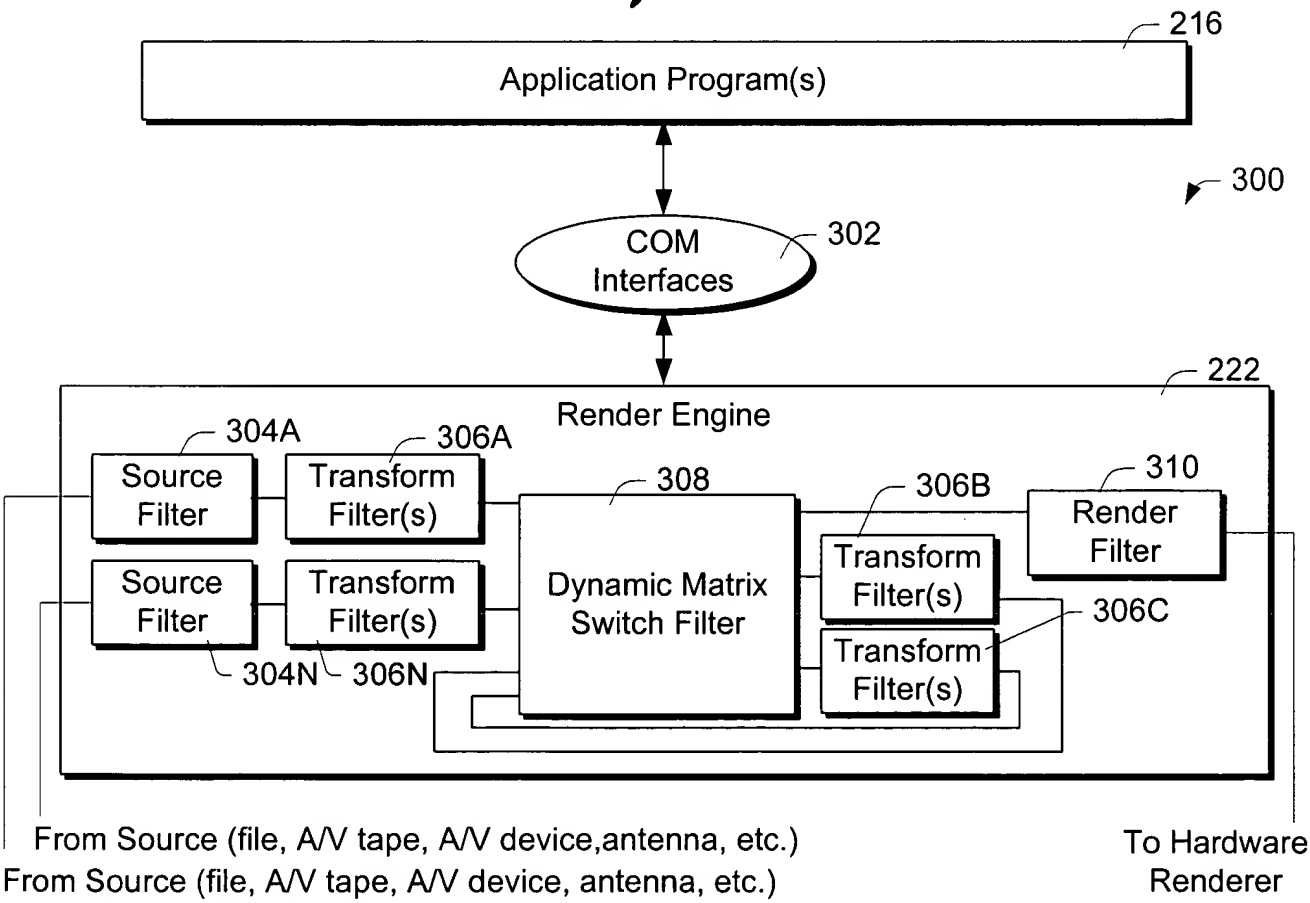


Fig. 3



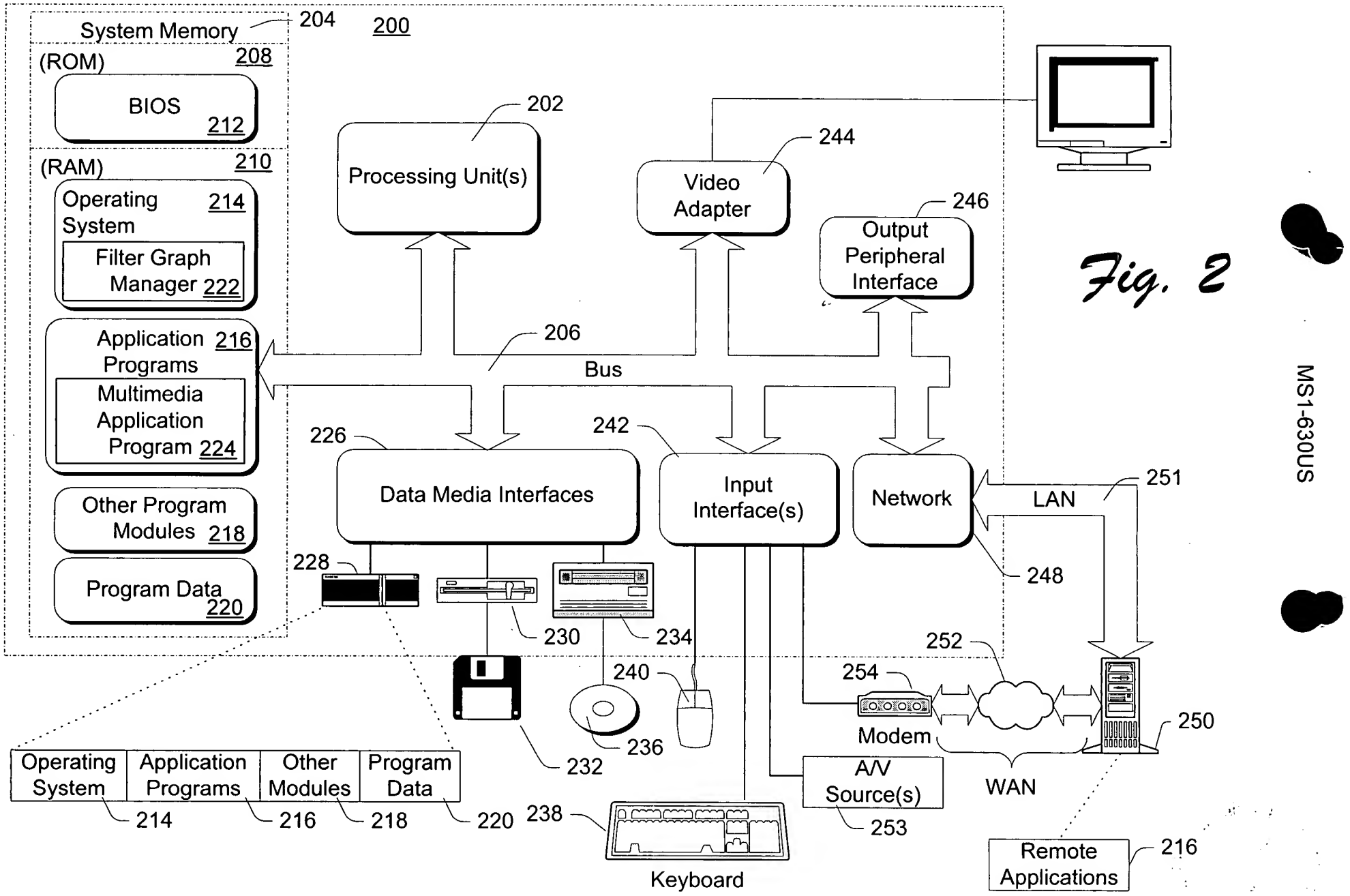

System Memory
204
200
(ROM)
208
BIOS
212
(RAM)
210
Operating System
214
Filter Graph Manager
222
Application Programs
216
Multimedia Application Program
224
Other Program Modules
218
Program Data
220
Processing Unit(s)
202
Video Adapter
244
Output Peripheral Interface
246
Bus
206
Data Media Interfaces
226
Input Interface(s)
242
Network
LAN
251
248
228
230
234
240
232
236
252
254
Modem
250
WAN
A/V Source(s)
253
238
Keyboard
Remote Applications
216
Operating System
214
Application Programs
216
Other Modules
218
Program Data
220

Fig. 2

Fig. 4

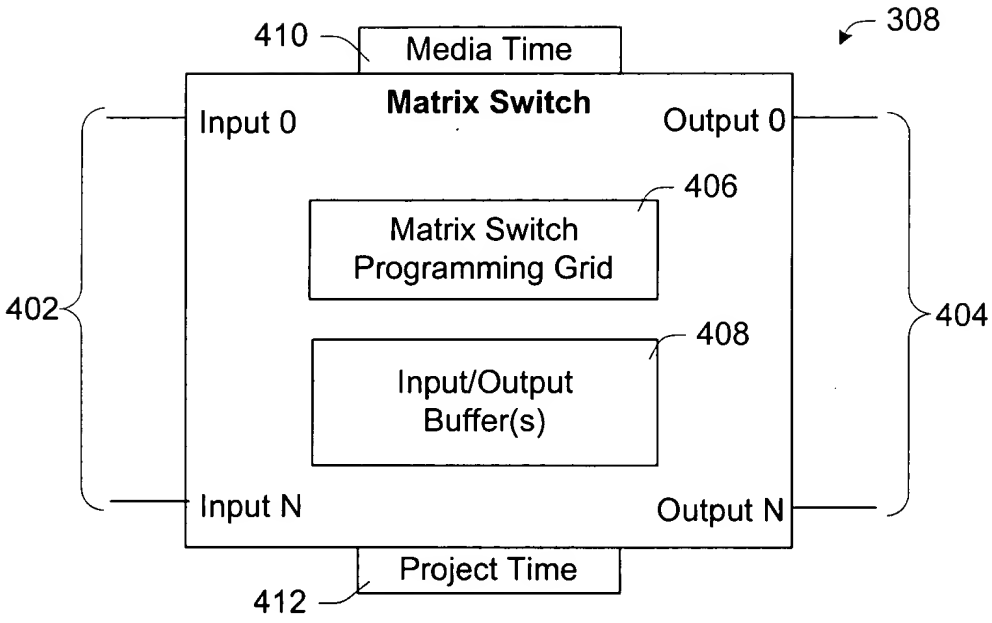

410
Media Time
308
Matrix Switch
Input 0
Output 0
406
Matrix Switch
Programming Grid
402
404
408
Input/Output
Buffer(s)
Input N
Output N
Project Time
412

Fig. 5

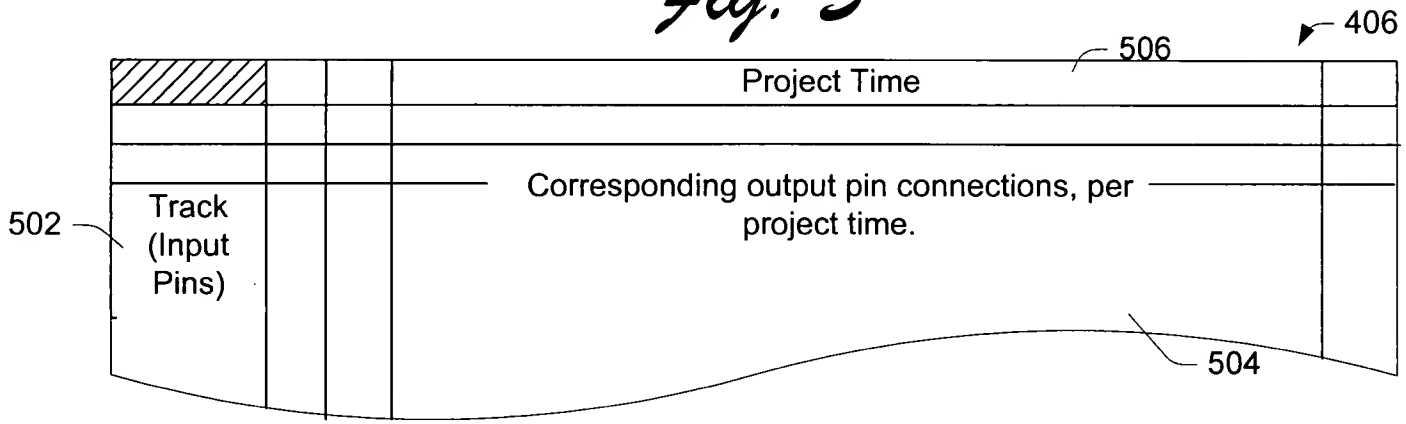

406
506
Project Time
Corresponding output pin connections, per project time.
502
Track (Input Pins)
504

Fig. 6

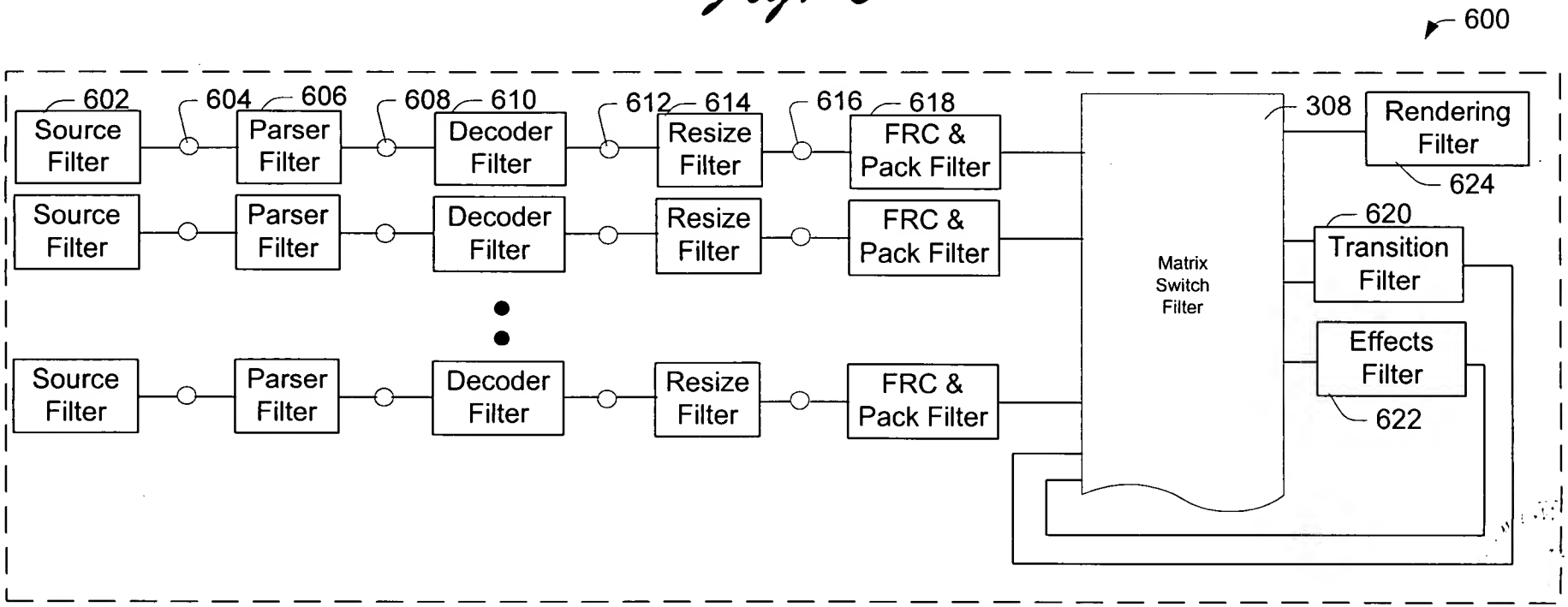

600
602
604
606
608
610
612
614
616
618
Source Filter
Parser Filter
Decoder Filter
Resize Filter
FRC & Pack Filter
Source Filter
Parser Filter
Decoder Filter
Resize Filter
FRC & Pack Filter
Source Filter
Parser Filter
Decoder Filter
Resize Filter
FRC & Pack Filter
Matrix Switch Filter
308
Rendering Filter
624
620
Transition Filter
Effects Filter
622

Fig. 7

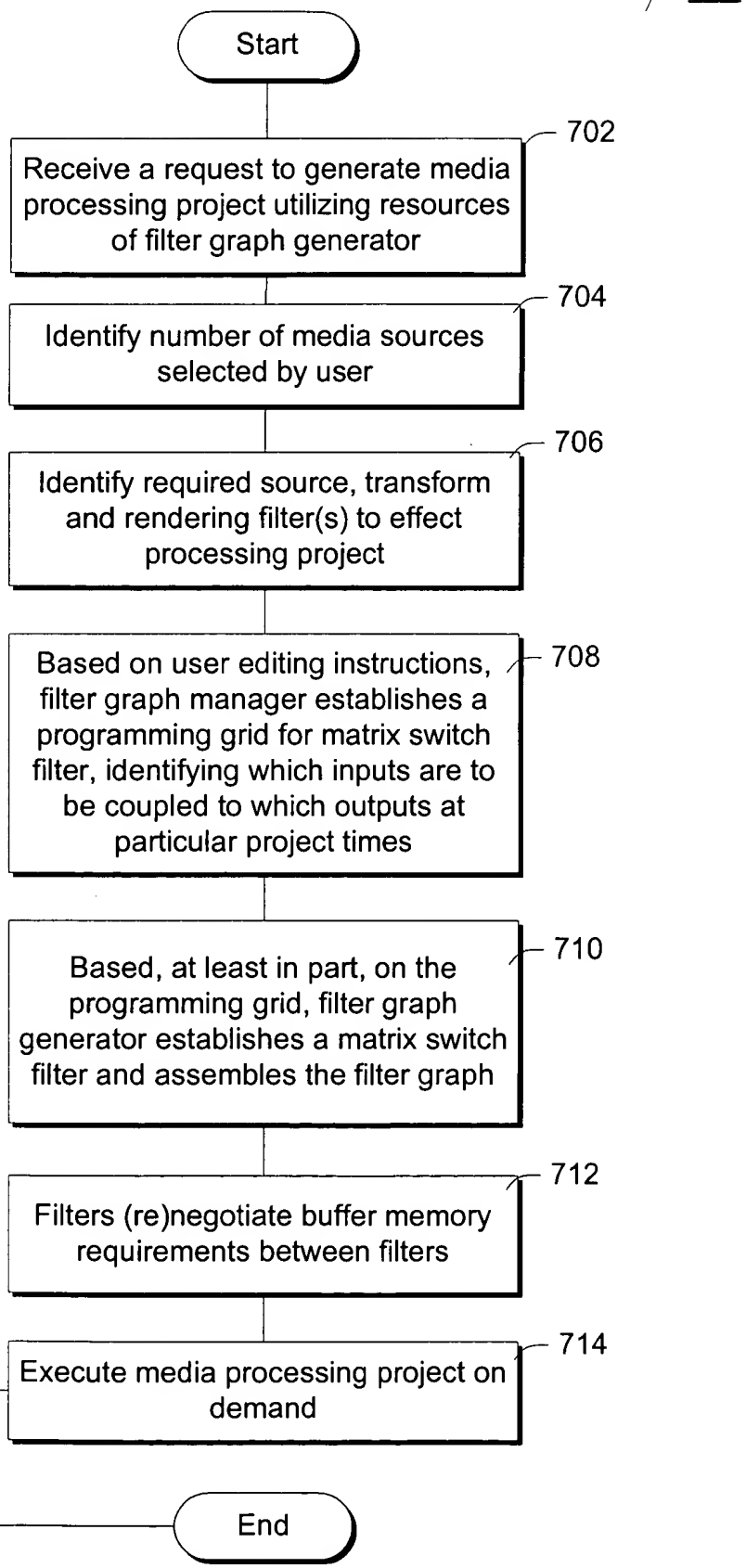
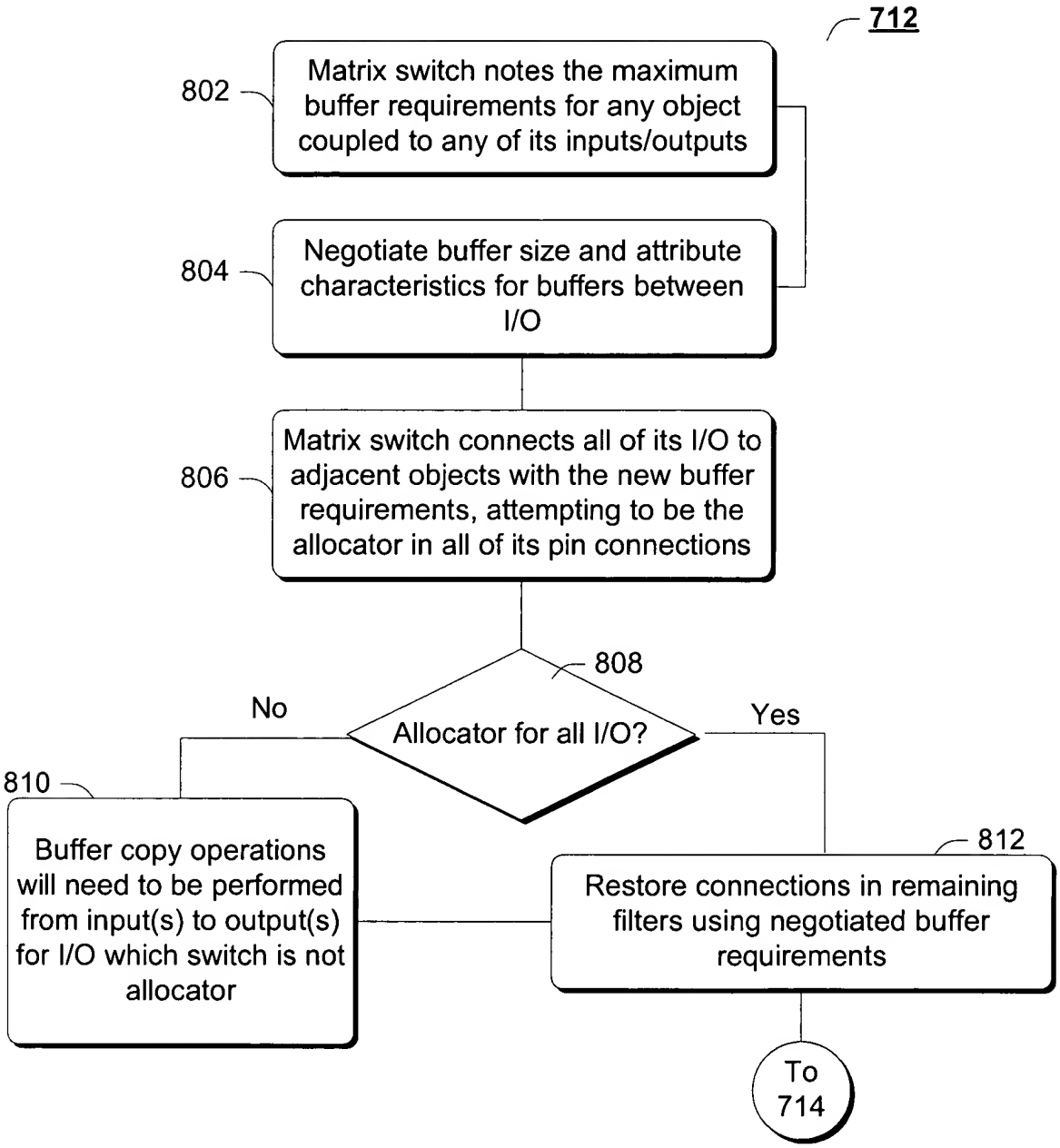

700
Start
Receive a request to generate media processing project utilizing resources of filter graph generator
702
Identify number of media sources selected by user
704
Identify required source, transform and rendering filter(s) to effect processing project
706
Based on user editing instructions, filter graph manager establishes a programming grid for matrix switch filter, identifying which inputs are to be coupled to which outputs at particular project times
708
Based, at least in part, on the programming grid, filter graph generator establishes a matrix switch filter and assembles the filter graph
710
Filters (re)negotiate buffer memory requirements between filters
712
Execute media processing project on demand
714
End

Fig. 8


712
802
Matrix switch notes the maximum buffer requirements for any object coupled to any of its inputs/outputs
804
Negotiate buffer size and attribute characteristics for buffers between I/O
806
Matrix switch connects all of its I/O to adjacent objects with the new buffer requirements, attempting to be the allocator in all of its pin connections
808
Allocator for all I/O?
No
Yes
810
Buffer copy operations will need to be performed from input(s) to output(s) for I/O which switch is not allocator
812
Restore connections in remaining filters using negotiated buffer requirements
To 714

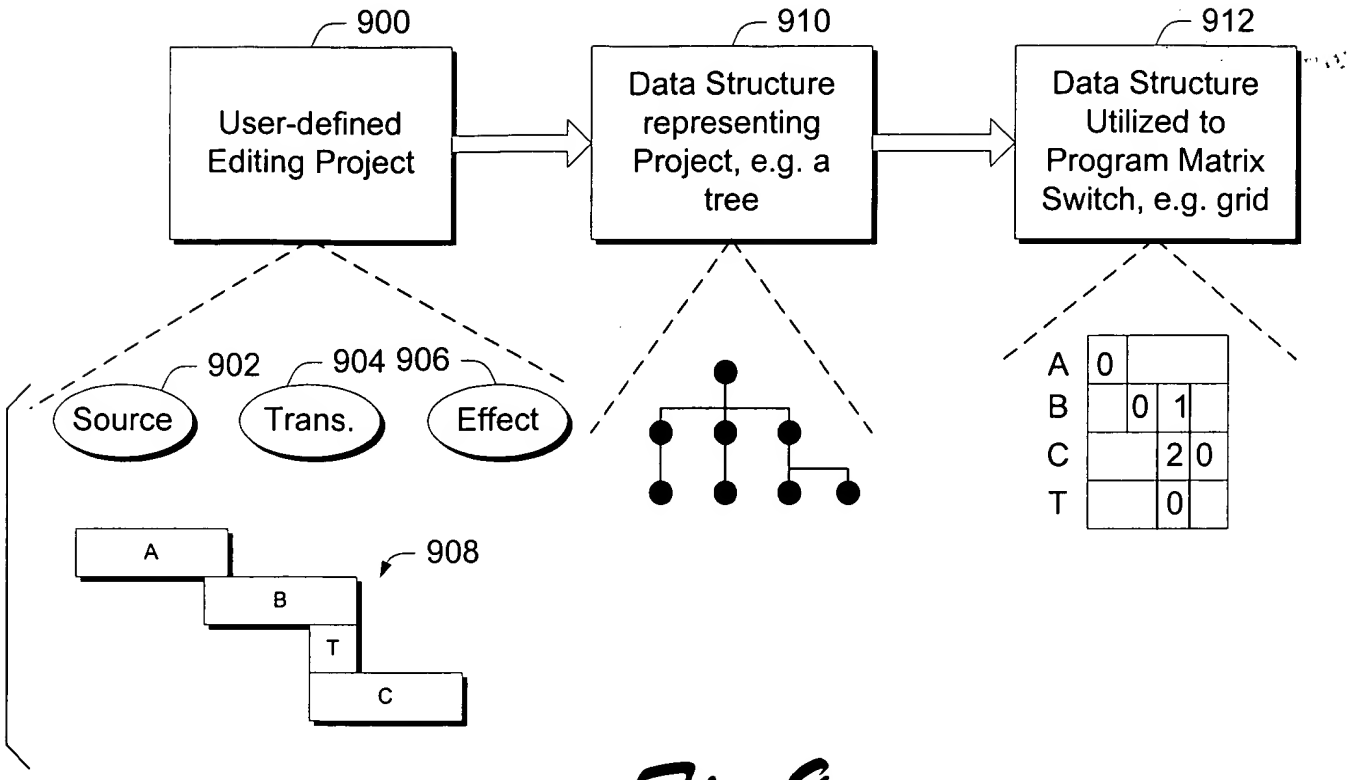

900
User-defined Editing Project
910
Data Structure representing Project, e.g. a tree
912
Data Structure Utilized to Program Matrix Switch, e.g. grid
902
Source
904
Trans.
906
Effect
A
B
T
C
908
A 0
B 0 1
C 2 0
T 0

Fig. 9

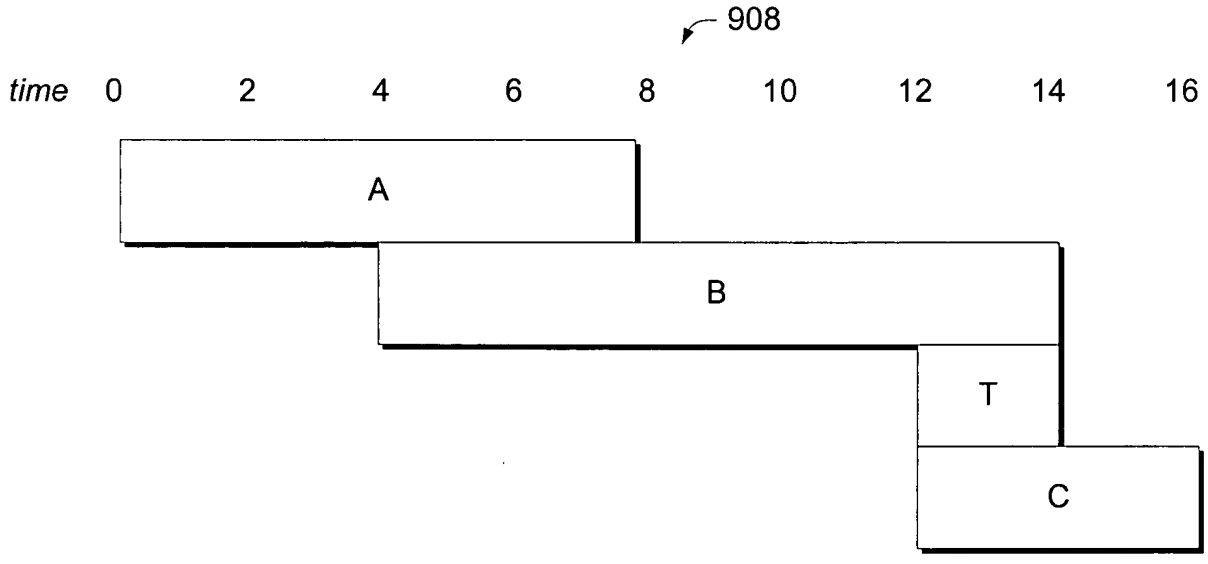

908
time 0 2 4 6 8 10 12 14 16
A
B
T
C

Fig. 10

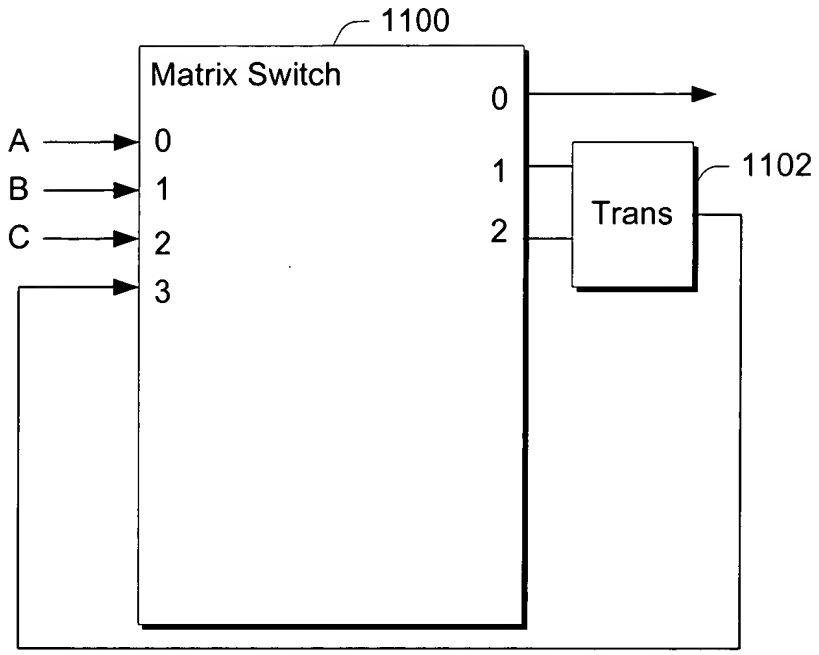

1100
Matrix Switch
A
B
C
0
1
2
3
0
1
2
Trans
1102

Fig. 11

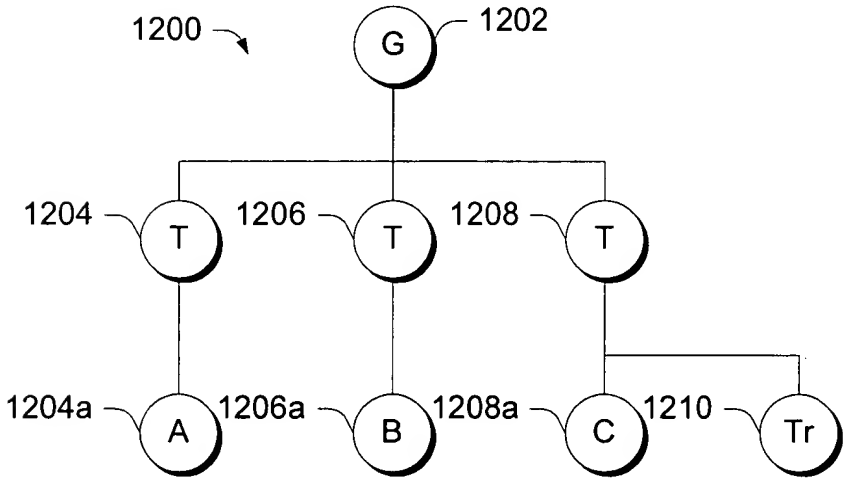

1200
G
1202
1204
T
1206
T
1208
T
1204a
A
1206a
B
1208a
C
1210
Tr

Fig. 12

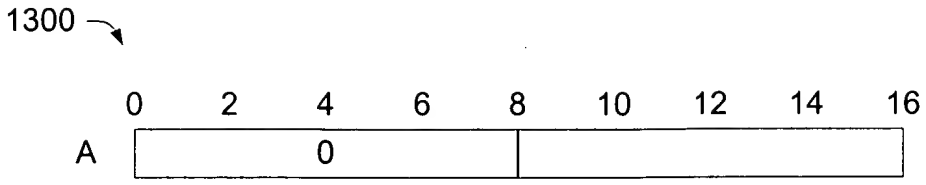


Fig. 13

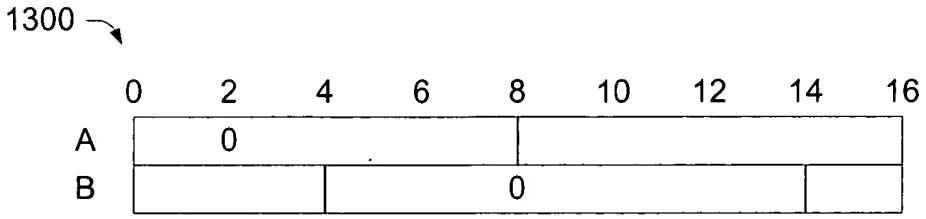


Fig. 14

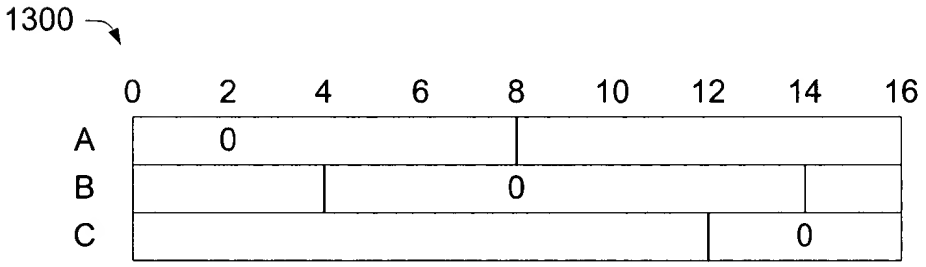


Fig. 15

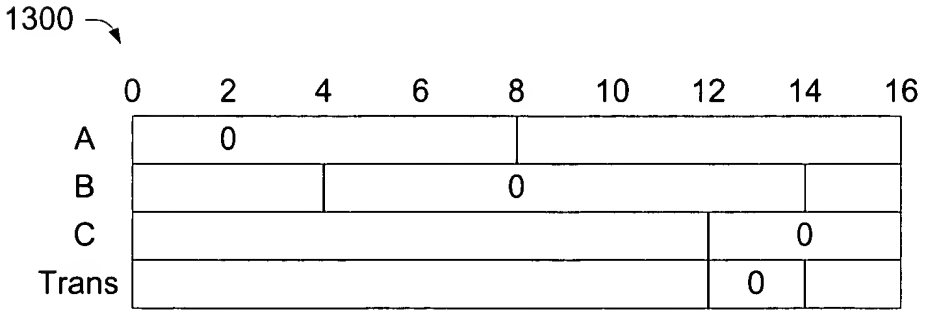


Fig. 16

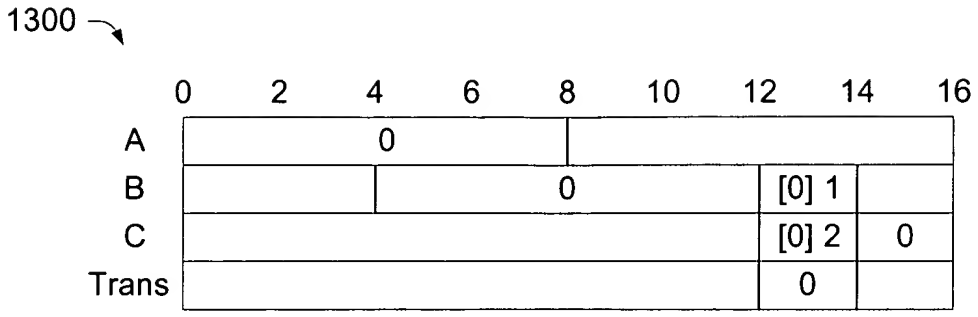

1300
0 2 4 6 8 10 12 14 16
A
B
C
Trans
0
0
[0] 1
[0] 2
0
0

Fig. 17

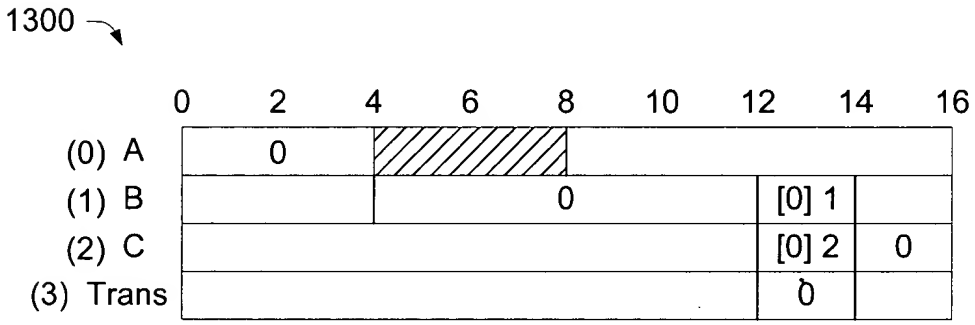

1300
0 2 4 6 8 10 12 14 16
(0) A
(1) B
(2) C
(3) Trans
0
0
[0] 1
[0] 2
0
0

Fig. 18

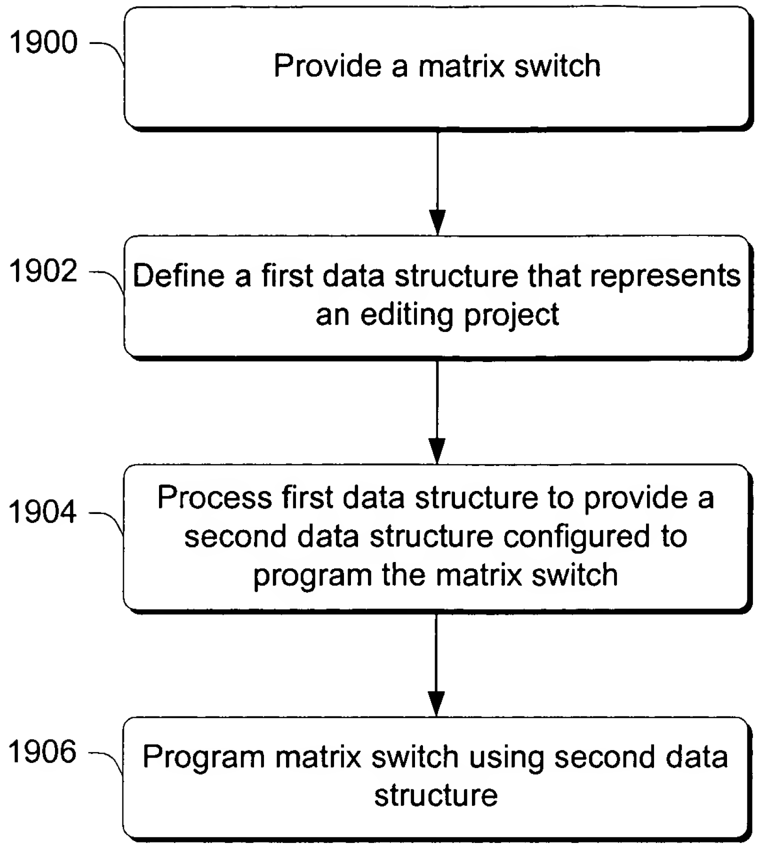

1900
Provide a matrix switch
1902
Define a first data structure that represents an editing project
1904
Process first data structure to provide a second data structure configured to program the matrix switch
1906
Program matrix switch using second data structure

Fig. 19

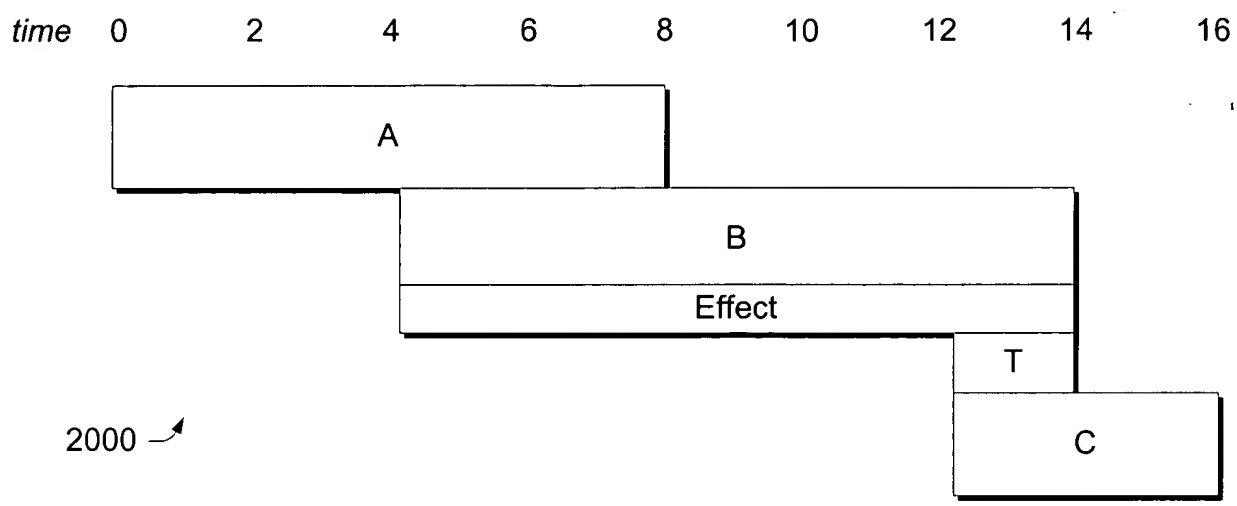


Fig. 20

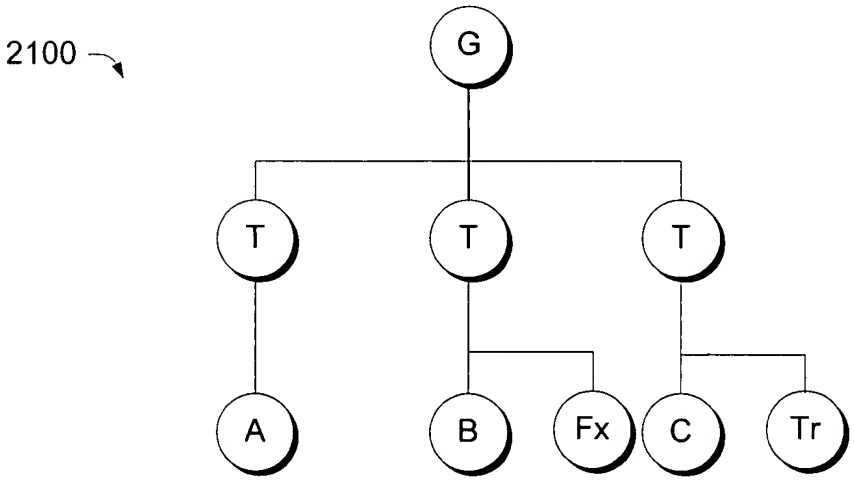


Fig. 21

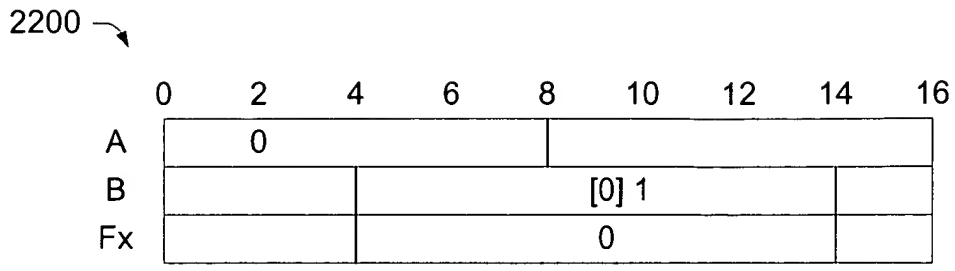


Fig. 22

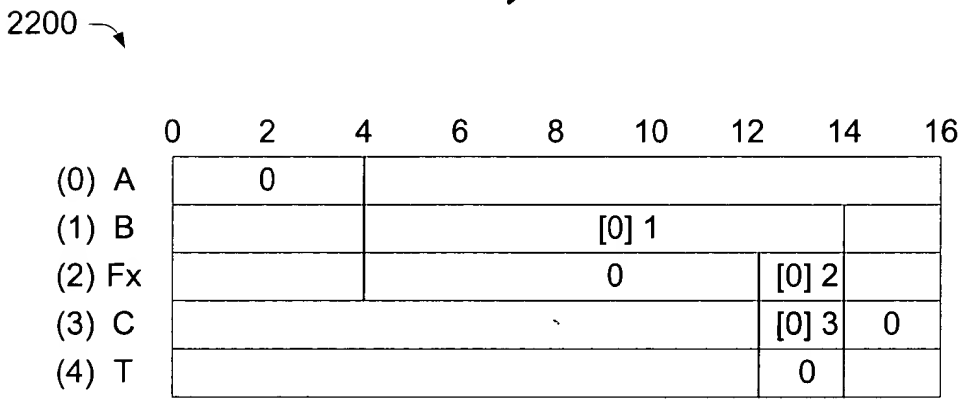


Fig. 23

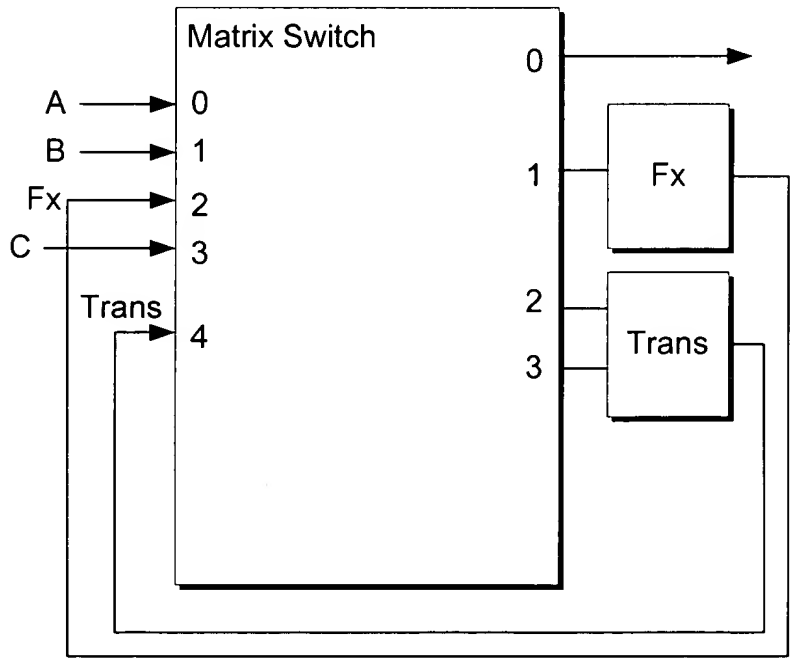


Fig. 24

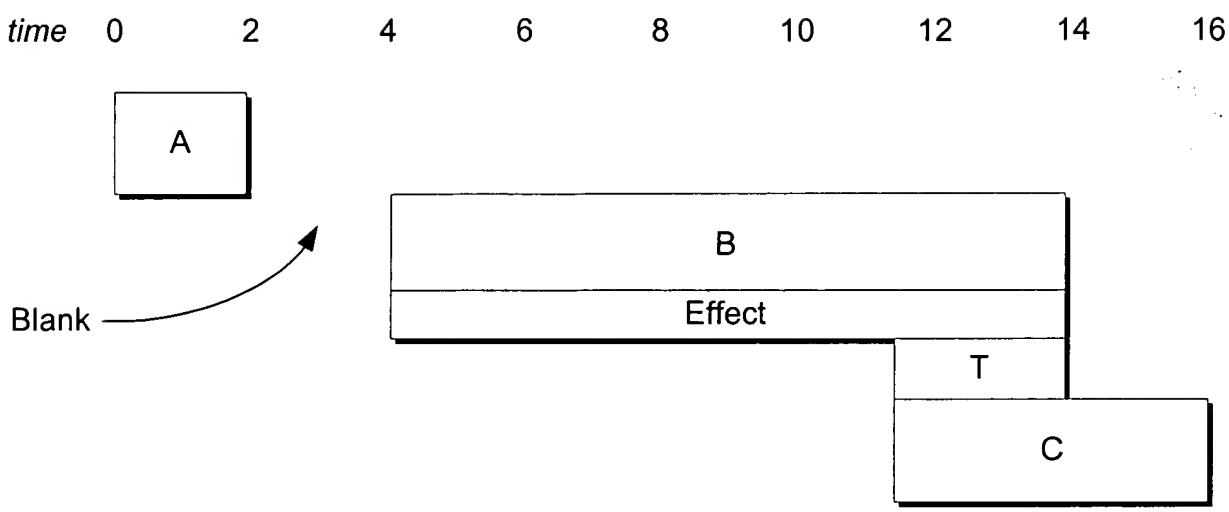

time
0
2
4
6
8
10
12
14
16
A
B
Effect
T
C
Blank

Fig. 25

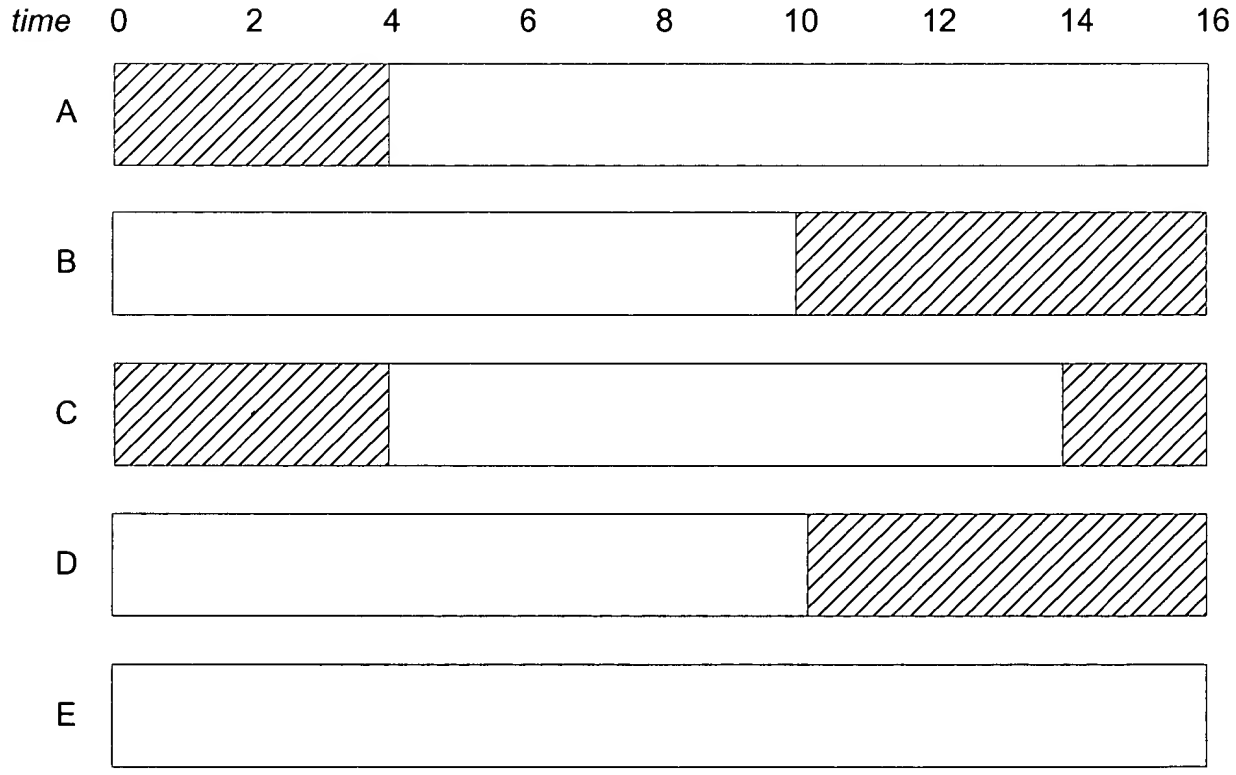

time
0
2
4
6
8
10
12
14
16
A
B
C
D
E

Fig. 26

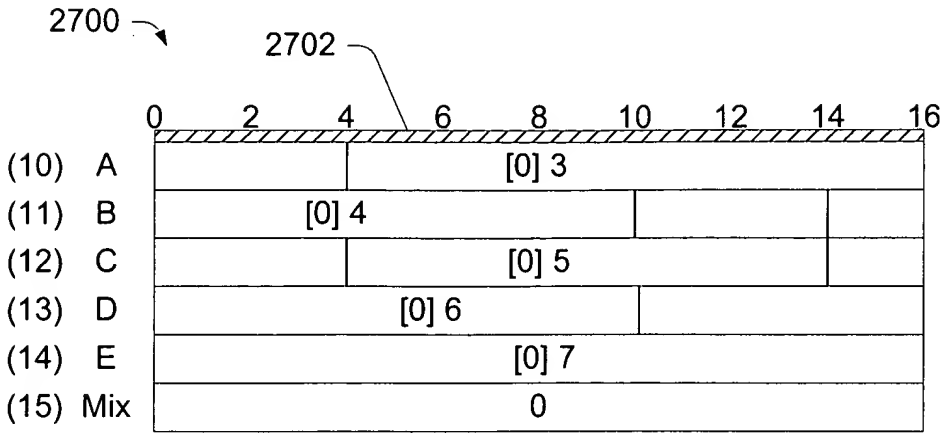

2700
2702
0 2 4 6 8 10 12 14 16
(10) A
(11) B
(12) C
(13) D
(14) E
(15) Mix
[0] 3
[0] 4
[0] 5
[0] 6
[0] 7
0

Fig. 27

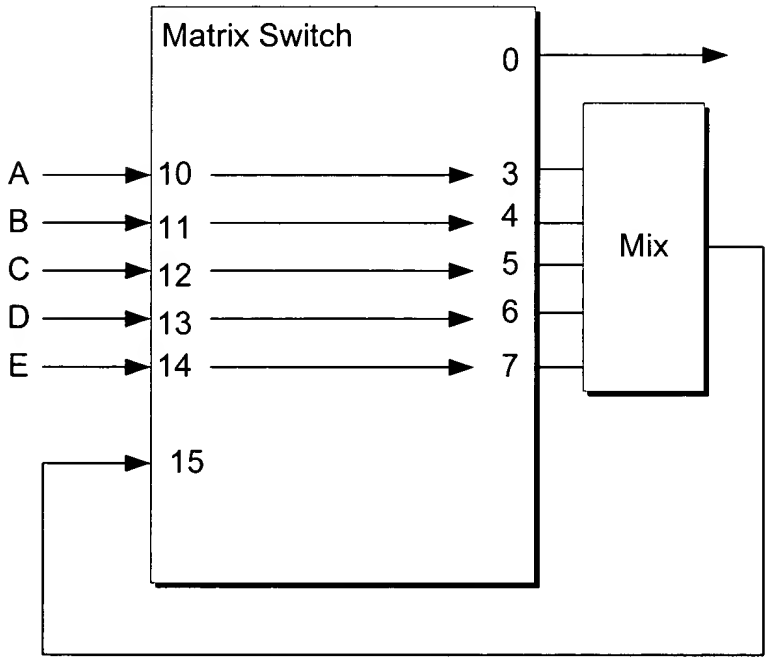

Matrix Switch
0
A
B
C
D
E
10
11
12
13
14
15
3
4
5
6
7
Mix

Fig. 28

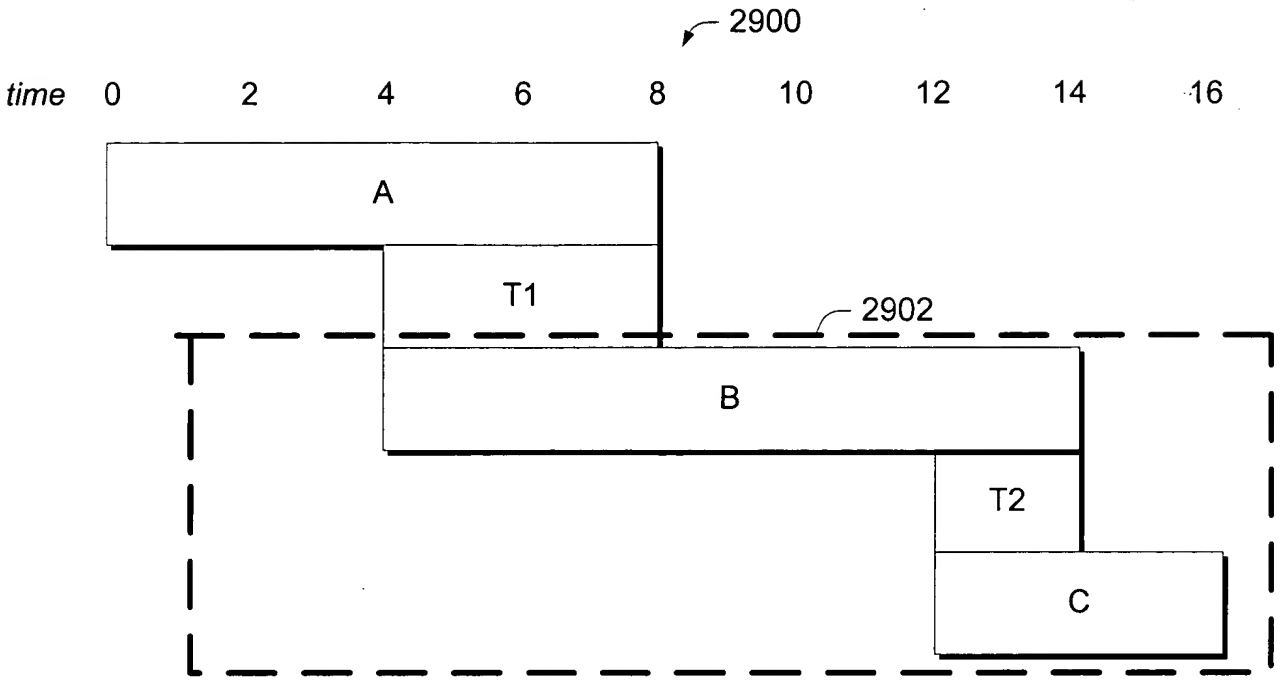

2900
time
0
2
4
6
8
10
12
14
16
A
T1
2902
B
T2
C

Fig. 29

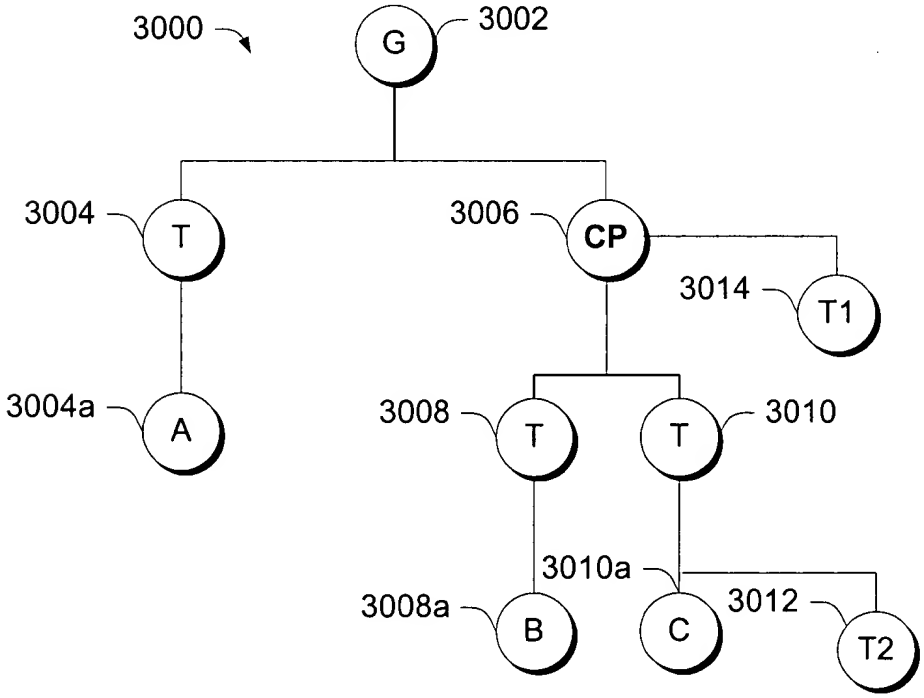

3000
G
3002
3004
T
3006
CP
3014
T1
3004a
A
3008
T
T
3010
3010a
3008a
B
C
3012
T2

Fig. 30

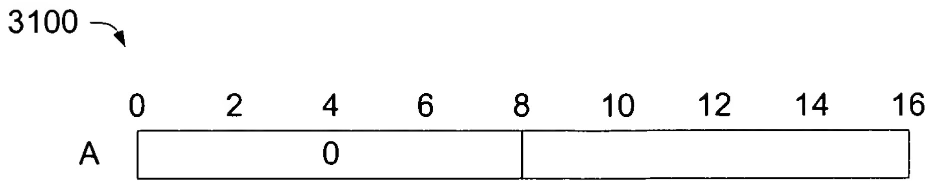


Fig. 31

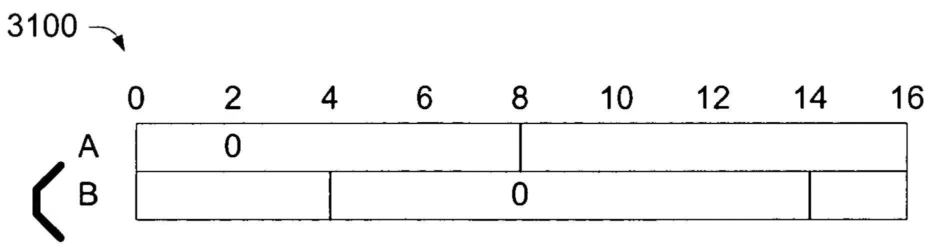


Fig. 32

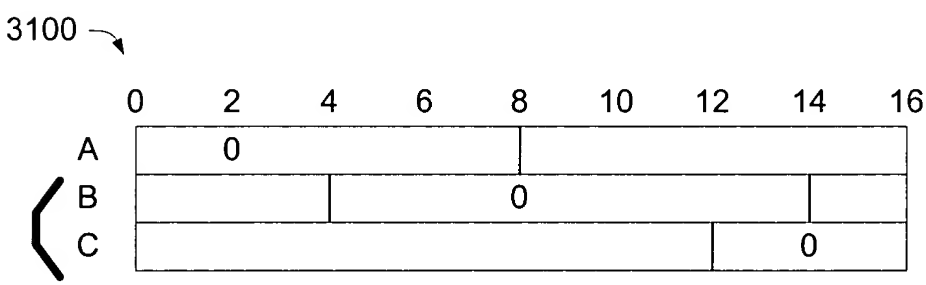


Fig. 33

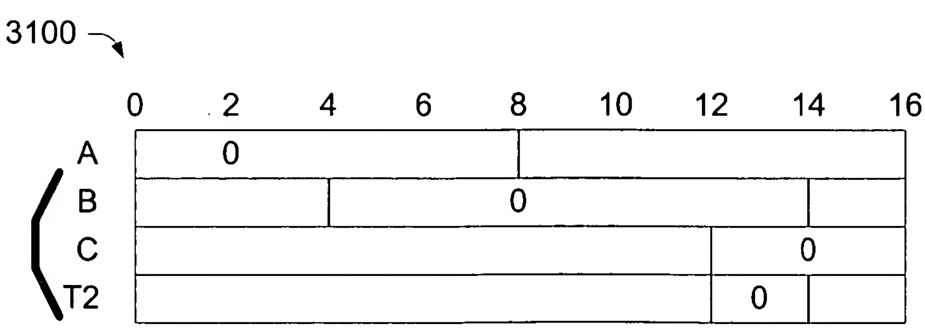


Fig. 34

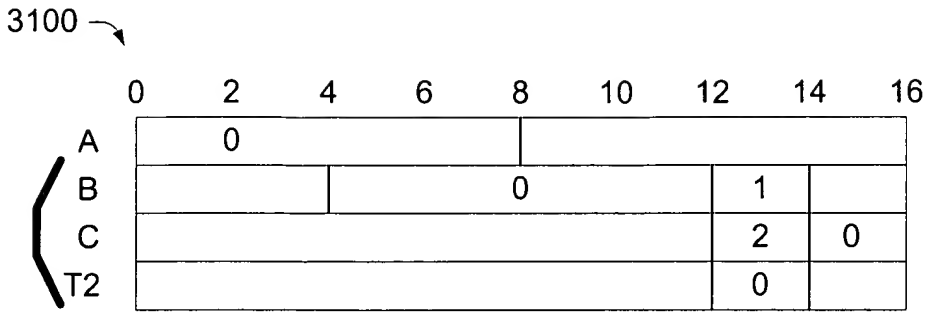


Fig. 35

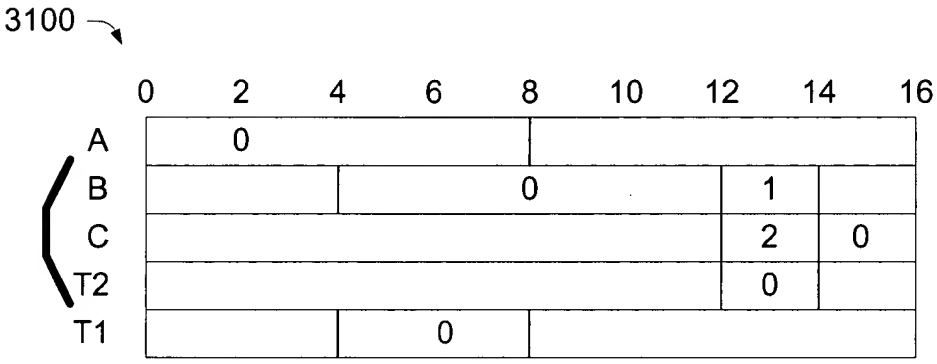


Fig. 36

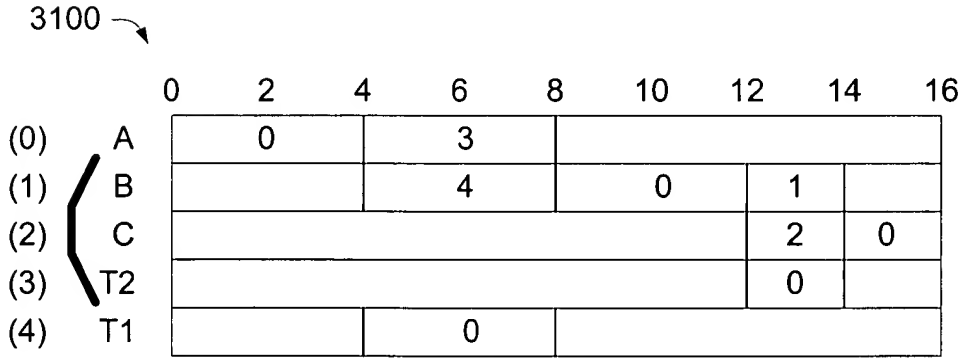


Fig. 37

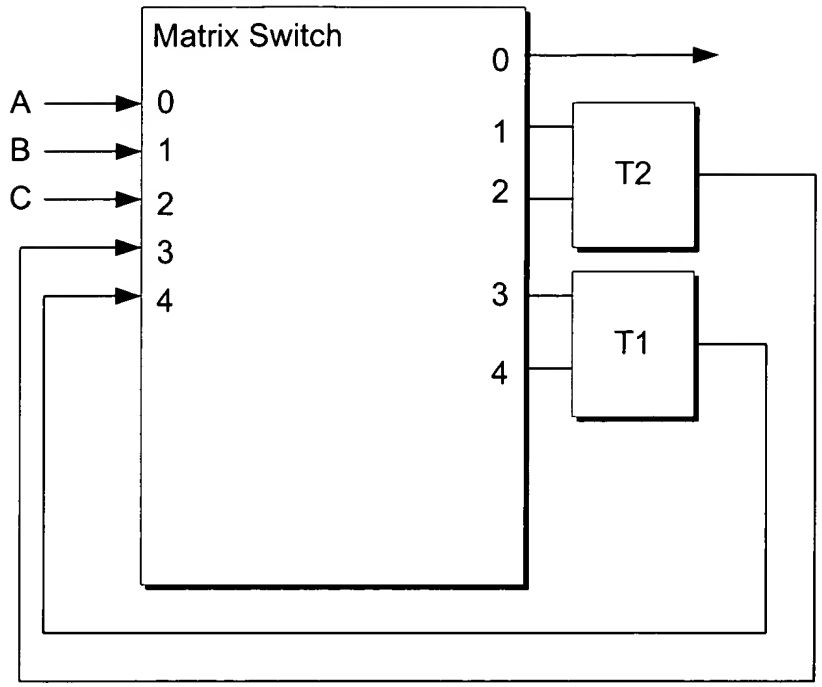


Fig. 38

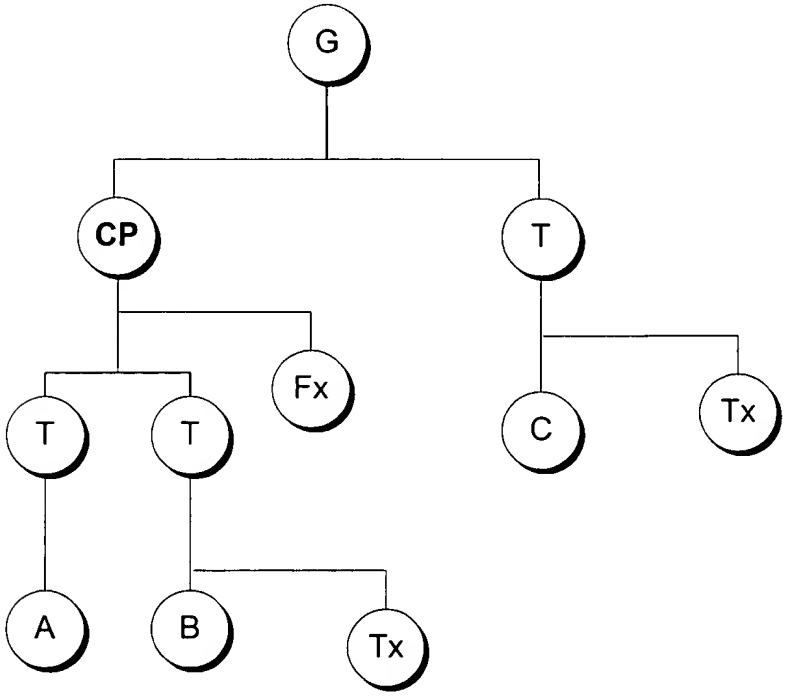


Fig. 38a

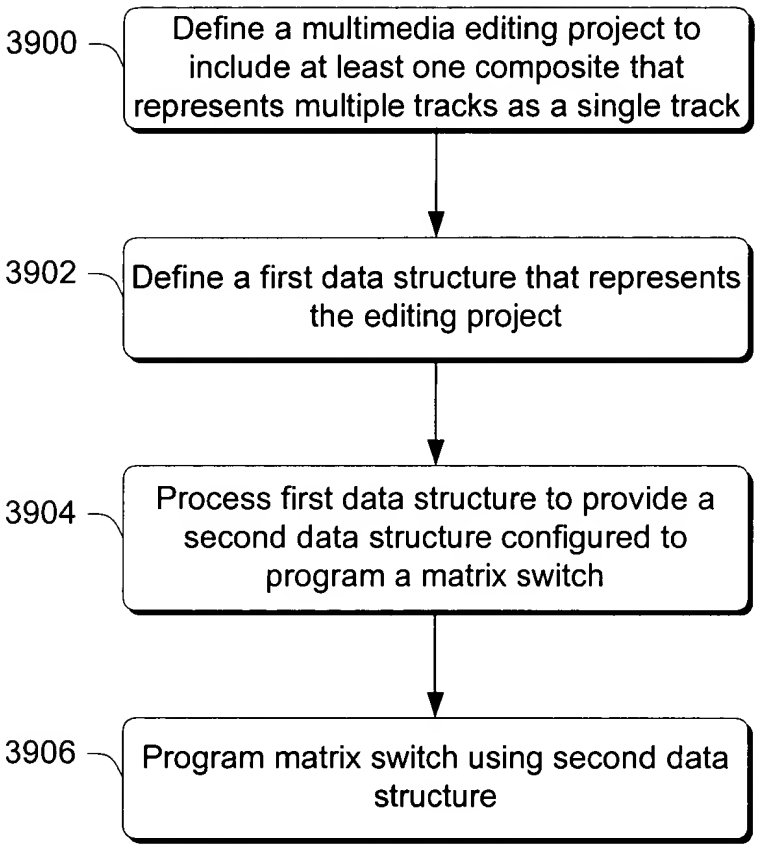

3900
Define a multimedia editing project to include at least one composite that represents multiple tracks as a single track
3902
Define a first data structure that represents the editing project
3904
Process first data structure to provide a second data structure configured to program a matrix switch
3906
Program matrix switch using second data structure

Fig. 39

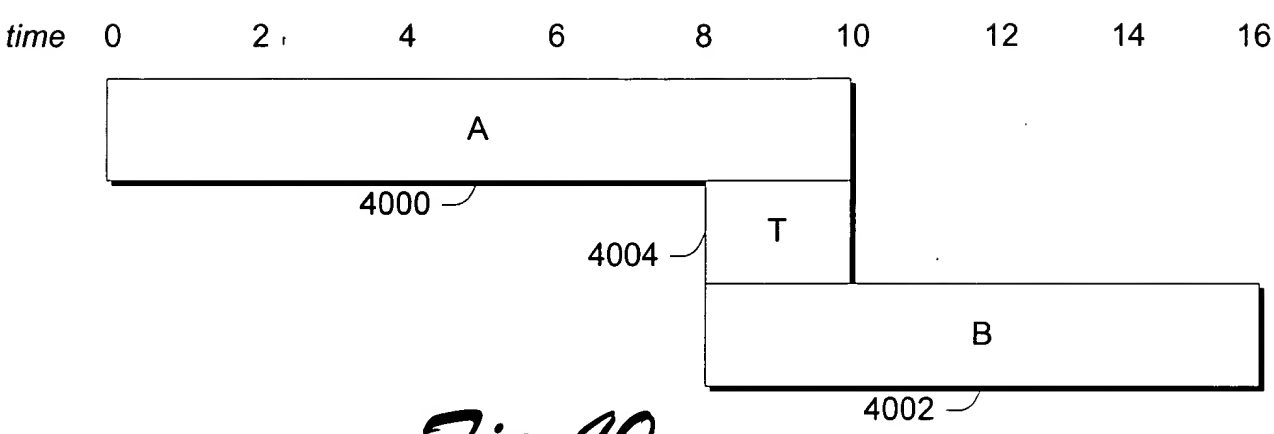

time
0
2
4
6
8
10
12
14
16
A
4000
T
4004
B
4002

Fig. 40

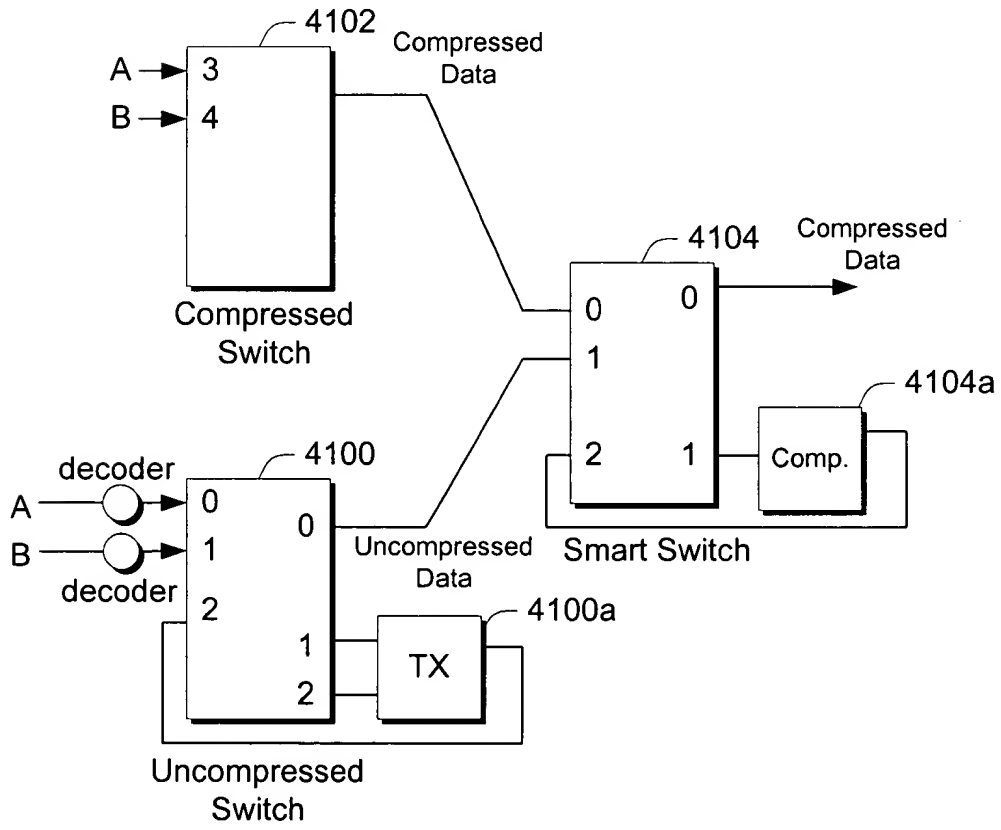

4102
A
B
3
4
Compressed Data
Compressed Switch
4104
Compressed Data
0
1
2
0
1
4104a
Comp.
decoder
A
B
decoder
4100
0
1
2
0
1
2
Uncompressed Data
Smart Switch
4100a
TX
Uncompressed Switch

Fig. 41

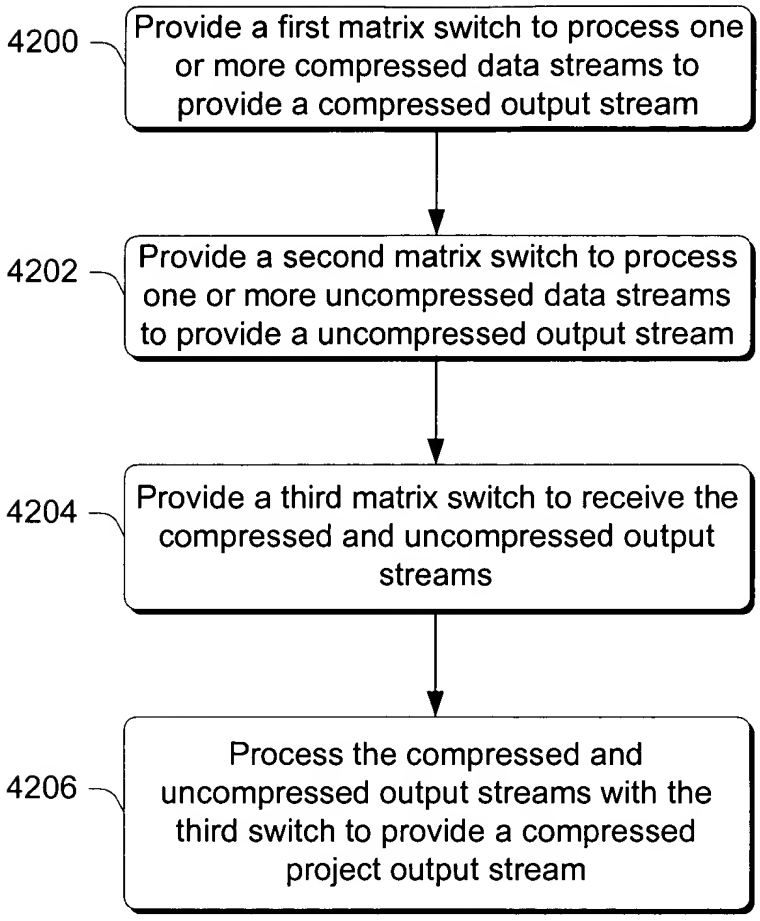
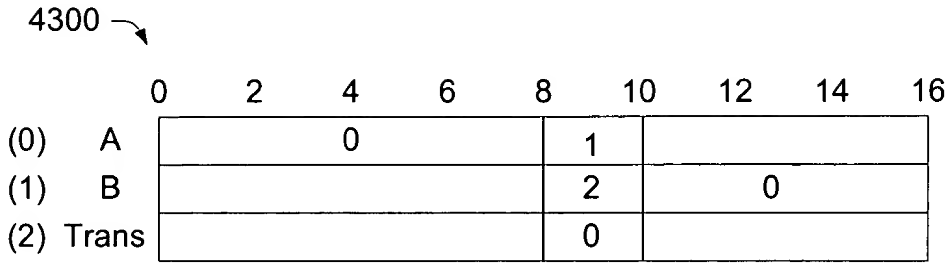
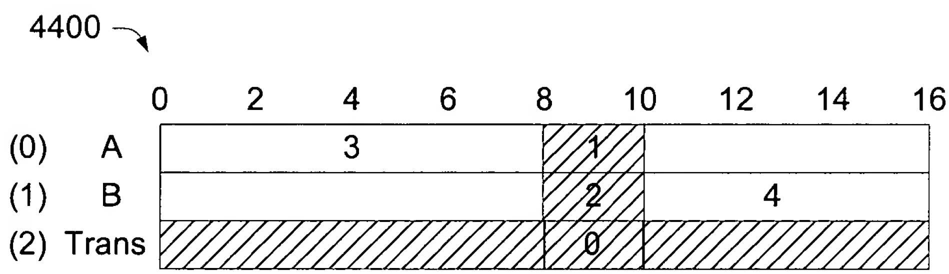

4200
Provide a first matrix switch to process one or more compressed data streams to provide a compressed output stream
4202
Provide a second matrix switch to process one or more uncompressed data streams to provide a uncompressed output stream
4204
Provide a third matrix switch to receive the compressed and uncompressed output streams
4206
Process the compressed and uncompressed output streams with the third switch to provide a compressed project output stream

Fig. 42



Grid for Uncompressed Project Portion

Fig. 43



Grid for Compressed Project Portion

Fig. 44

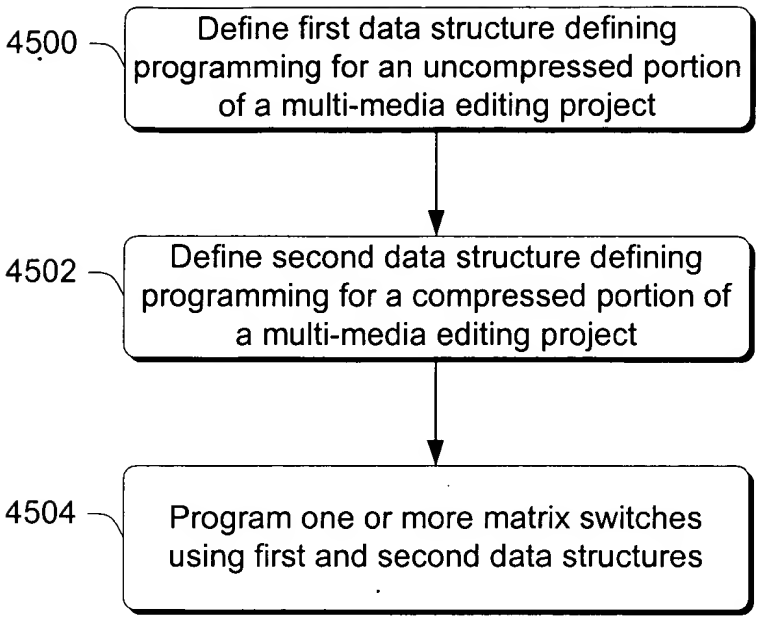


Fig. 45